EPTC 2017 Panel Session

Packaging Challenges & Opportunities of 5G-mm Wave Technology

Moderator : ***Dr. Rick Sturdivant***, Department of Engineering and Computer Science, Azusa Pacific University, USA.

Dr. Rick Sturdivant is a recognized expert in the field of electronic packaging, transmit/receive modules, and phased arrays. He is coeditor of *RF and Microwave Microelectronics Packaging II* (Springer Publishing, 2017), coauthor of *Transmit Receive Modules for Radar and Communication Systems* (Artech House, 2015), coauthor of *Hands On Guide To Heat Transfer For Microwave and Millimeter-wave Electronics* (Amazon.com eBook, 2015), and author of *Microwave and Millimeter-wave Electronic Packaging* (Artech House, 2013). He has also contributed several book chapters, numerous journal papers and conference papers. He holds seven U.S. patents. From 1989 to 2000 he engineered transmit receive modules for Hughes/Raytheon where he received the engineering excellence award for developing the world's first tile array module. Since the year 2000, he has started several successful technology companies providing solutions for wireless, microwave, millimeter-wave, and high-speed products. He is an Assistant Professor at Azusa Pacific University Founder and Chief Technology Officer of MPT, Inc.

He earned the Ph.D. degree from Colorado State University, M.A. degree from Biola University, M.S.E.E. degree from the University of California at Los Angeles, B.S.E.E. degree from the California State University at Long Beach, and the B.A. degree from Vanguard University. For more up to date information, visit his website at ricksturdivant.com.

<u>Panel Speaker #1</u> : ***Dr. Rajendra Pendse*, Senior director, R&D, Qualcomm**

Title : 5G - Implications for Packaging Technology

Dr. Raj Pendse leads Packaging Strategy at Qualcomm, covering core Packaging technology for Application Processors, Modems and RF/Analog devices and use cases in Mobile and adjacent markets like Automotive and Servers.

Prior to Qualcomm, Raj held leadership roles at STATSChipPAC (now JCET), Hewlett-Packard Labs and National Semiconductor, where his work

spanned the areas of Packaging for high-end microprocessors, ASIC's, GPU's and low-cost packaging solutions for Consumer hardware. His most recent focus has been on new Packaging for 5G which includes novel approaches like SoC partitioning, new Memory integration schemes and mm wave RF & antenna integration.

Raj completed his BS in Materials Science from IIT Bombay with Top in Class honors and his Doctorate in Materials Science from UC Berkeley.

<u>Panel Speaker #2</u> : ***Santosh Kumar,*** **Senior Technology and Market Analyst, Yole Development**

Title : Challenges and requirements for 5G packaging

Santosh Kumar is currently working as Senior Technology & Market Research Analyst at Yole Développement. He is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies. His main interest areas are advanced IC packaging technology including equipment & materials. He is the author of several reports on fan-out / fan-in WLP, flip chip, and 3D/2.5D packaging.

He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 40 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

<u>Panel Speaker #3</u> ***: Ranauld Perez*****, Marketing director, Johnstech International**

Title : The Elusive Happy Medium: mm Wave Device Packaging vs Cost of Test

Current Responsibility:
Director of Marketing, Sales and Business Development – Johnstech International (Minneapolis, MN)

Past Affiliations:
Business Director, Maxim Integrated, Mobile Power

Marketing Director, R2 Semiconductor, RF Power
Senior Product Marketing Manager at National Semiconductor and Skyworks Solutions
Product Engineering Manager, International Rectifier
Education : BSEE/MS, BSManagement

Panel Speaker #4 *: Eldon Staggs* **, ANSYS Inc, USA**

Title：Modeling and Simulation Challenges in the mmWave regime

Abstract ： As the never ending pursuit to push the limits in size, performance and functionality into a smaller space continues, modeling and simulation best practices need to be explored. We will look at simulation challenges and technologies best suited to capture and explore next generation packaging technologies. Fundamental governing electromagnetic equations are used to investigate what is expected and what was not expected for a given construct.

Eldon Staggs is a Principal Engineer for Ansys, Inc. with specialization in high-frequency electromagnetics, circuit and system design. He works with

Ansys' top tier customers on their high frequency designs. Eldon has 27 years of design experience and is very knowledgeable in system, RF, analog, and digital engineering for electronic warfare and electronic intelligence systems. He earned his BSEE degree from the University of New Mexico in Albuquerque, NM, and his MSEE degree from the University of California at San Diego.

<u>Panel Speaker #5</u> ***: Dr. Surya Bhattacharya,*** **Director of Industry Development, A*STAR Institute of Microelectronics (IME), Singapore**

Title : Fan-Out Packaging For 5G and mmWave Applications

Dr. Surya Bhattacharya is Director, Interconnect & Packaging Platform for A*STAR Institute of Microelectronics (IME). Surya has over 20 years of experience in CMOS technology development while working in the US semiconductor industry at both Fabless companies and Integrated Device Manufacturers(IDM). He joined IME in 2011 from Qualcomm CDMA Technologies, San Diego, California, a world leader in semiconductor chips for 3G and LTE mobile phone markets. At Qualcomm, he served as Director of Foundry Engineering while he oversaw technology and

manufacturing ramps across multiple foundries in Asia and around the world. Prior to Qualcomm, he was a Principal Foundry Engineer at Broadcom Corporation, Irvine, California, driving CMOS development and manufacturing for Broadcom's networking and wireless products at Asian foundries. He started his career at Rockwell Semiconductor Systems, Newport Beach, California, where he was Senior Manager for CMOS technology development for Rockwell's communication products. Surya obtained his Ph.D from the University of Texas, Austin, and B. Tech degree from the Indian Institute of Technology Madras.